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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,135	PATEL ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-11* is/are allowed.

6)☒ Claim(s) *1,5,6,12,14,15,17-20 and 22-24* is/are rejected.

7)☒ Claim(s) *2-4,13,16,21 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *30 December 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because they fail to label the reference numerals according to their functions, all of the reference numerals require a corresponding textual label in addition to the numeric label. For example, reference numeral 404 in Fig. 9 should be labeled as --Phase Detector-- as described in the specification (page 9). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are the structural and/or functional connections between the following elements: a network interface & one or more networks and the other elements of the integrated circuit in the claim.

Claims 18 and 19 are similar rejected; note the above discussion with regard to claim 17.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5, 6, 12, 14, 15, 20, and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saeki (US 6,621,317) in view of Ooishi (6,424,585).

With regard to claims 1, 12, 23, and 24, Saeki discloses in Figs. 15-24 an integrated circuit, and a method of use thereof, comprising a delay chain (10), which is capable of receiving an input signal (1; CLOCK) and producing multiple delayed signals (P0-P3) that represent delayed versions of the input signal, wherein the multiple delayed signals are separated by a first phase increment (T/4); multiple interpolator blocks (30_1-30_n), operably coupled to the delay chain, wherein consecutive ones of the multiple interpolator blocks are capable of receiving and interpolating between consecutive ones of the multiple delayed signals to produce an interpolated

version of the input signal, wherein the interpolated version is delayed to one of multiple, intermediate delay values that are separated by a second phase increment that is smaller than the first phase increment; and a current source select signal generator circuit (40), operably coupled to the multiple interpolator blocks, and which is capable of providing variable current source select signals (PHs) to the multiple interpolator blocks to control interpolation between the consecutive ones of the multiple delayed signals. The circuit of Saeki meets all of the claimed limitations of the claimed circuit except that Saeki does not disclose details of the current source select signal generator circuit, which includes a split current source, as recited in the claim. Ooishi teaches in Fig. 22 a circuit having function of a current source select signal generator circuit which is capable of providing variable current source select signal (VCI), and including a split current source (N5). Therefore, it would have been obvious to one of ordinary skill in the art to replace the current source select signal generator circuit of Saeki with the circuit taught by Ooishi in order to provide stable voltage signals to the multiple interpolator blocks.

With regard to claim 5, the first phase increment is approximately equal to $(1/F_{MAX}) / N$ (see Fig. 17 of Saeki).

With regard to claim 6, the above discussed circuit of the references meets all of the claimed limitations except for specifying that the second phase increment is approximately equal to $(1/ F_{MAX}) / N*M$), wherein F_{MAX} equals a maximum frequency of the input signal, N equals a number of delay chain stages, and M equals a number of intermediate phase delays. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to set the second phase increment to meet the specific condition of the particular application since the second phase increment can be varied (see column 18, lines 45-64 of

Saeki). It has been held that discovering an optimum range or to optimally match to an application is obvious to the skilled artisan. See *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

With regard to claims 14 and 22, the integrated circuit further comprises logic circuitry (50), which is capable of producing a delay value signal (OUT), wherein the delay value signal indicates which two blocks of the multiple interpolator blocks (30_1-30_n) are to be used as the consecutive interpolator blocks from which the interpolated version of the input signal is produced.

Claims 15 and 20 are similar rejected; note the above discussion with regard to claims 1 and 12. Furthermore, the limitation "system", in claim 15, is also met by Saeki. Since it is very obvious that the integrated circuit of Saeki is inherently included in a system which provides the clock signal (i.e., CLOCK in Fig. 24) to the integrated circuit, and receives the delayed output clock signal (OUT) from the integrated circuit. Moreover, the limitation "test assembly" is also met by Saeki (by given the broadest reasonable interpretation). That system can be considered as a test assembly.

Allowable Subject Matter

5. Claims 2-4, 13, 16, 21, and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 7-11 are allowed.

The prior art of record fails to disclose or fairly suggest a circuit (400 in instant Fig. 4) and a method of use thereof, as recited in claims 2, 13, 16, 21, and 25, having a very specific limitation as each of the multiple interpolator blocks (500-512 in instant Fig. 5) comprises an interpolator block current source (602 in instant Fig. 6) having a first number (PX [0:9]) of transistor legs, which are selectively activatable based on a value of an input bias signal (PBIAS) to the current source; and wherein the split current source of the current source select signal generator circuit (800 in instant Fig. 8) comprises a first current source (804) having a second number (P0 [0:4]) of transistor legs that is a first fraction of the first number; and a second current source (806) having a third number (P1 [5:9]) of transistor legs that is a second fraction of the first number; and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a circuit (400 in instant Fig. 4) and a method of use thereof, as recited in claim 4, having a very specific limitation as a differential comparator (530 in instant Fig. 5), operably coupled to the multiple interpolator blocks (500-512), which is capable of producing, as an output (532), the interpolated version of the input signal (420) based on signals (524, 526) received from the multiple interpolator blocks; and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a circuit (400 in instant Fig. 4) and a method of use thereof, as recited in claim 7, having a very specific limitation as each interpolator block (600 in instant Fig. 6) comprises an interpolator block current source (602) having a first number (PX[0:9]) of transistor legs, wherein a number of activated legs, at any

given time, is based on a variable current source select signal (PBIAS), and multiple input signal gates (606, 608), which are activatable in response to a multi-phase signal (DIN 0, DIN 0# - DIN 12, DIN 12#); and a current source select signal generator circuit (800 in instant Fig. 8), operably coupled to the multiple interpolator blocks (500-512 in instant Fig. 5), and which is capable of providing variable current source select signals to the consecutive ones of the multiple interpolator blocks, and wherein the current source select signal generator circuit includes a split current source (804, 806); and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

7. Regarding claims 17-19, the patentability thereof cannot be determined because of their indefiniteness.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ashuri (US 5,489,864) is cited as of interest because it discloses a delay interplation circuitry.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
February 14, 2005

TUAN T. LAM
PRIMARY EXAMINER